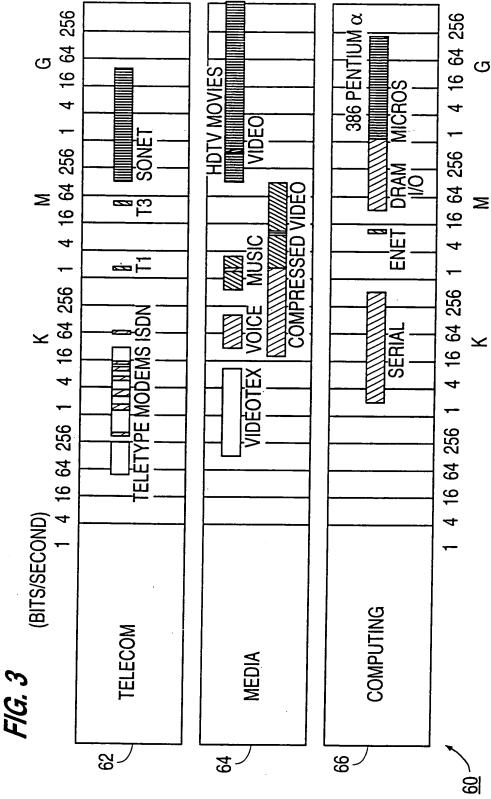


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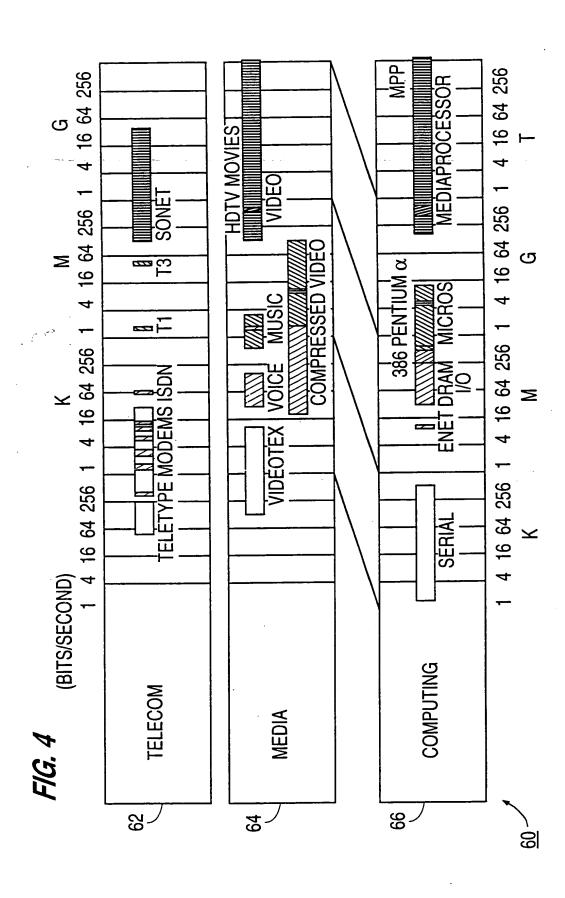
ON 10.



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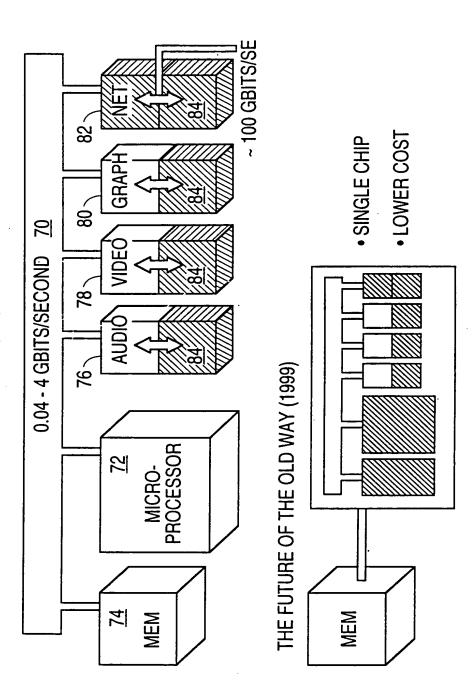
BY CLASS SUBCLASS

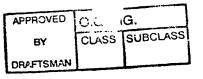
DRAFTSMAN

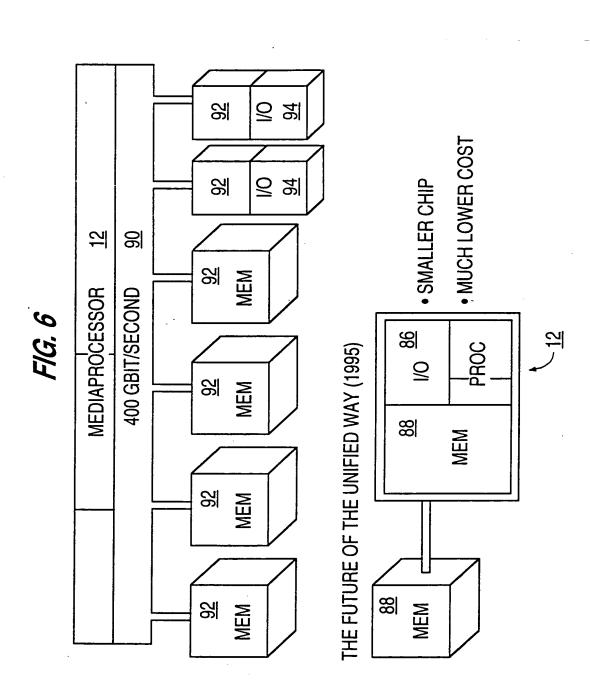


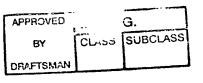
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		DRAFTSMAN

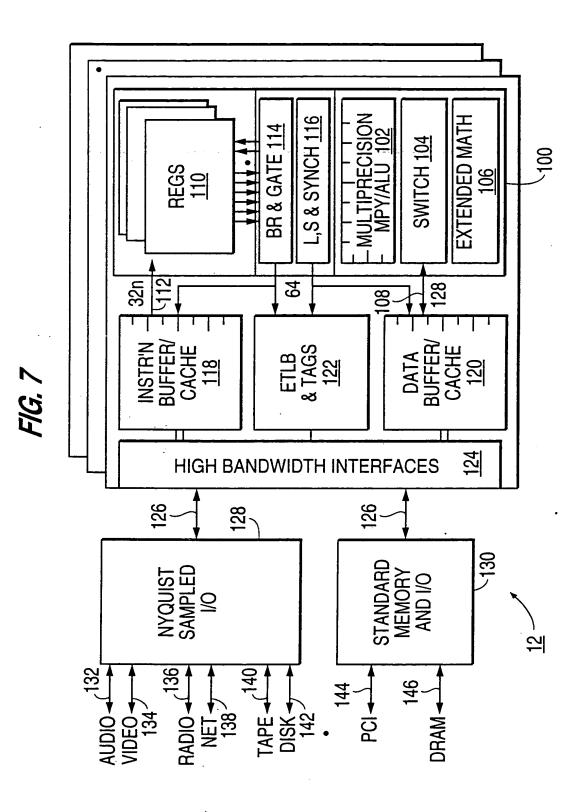
FIG. 5



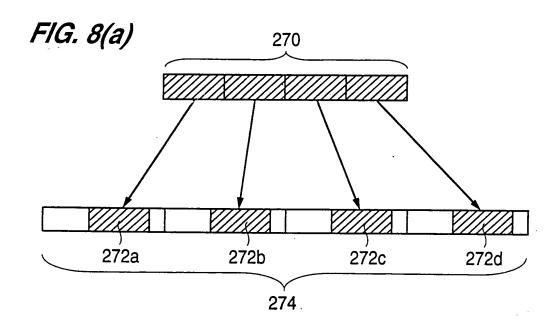


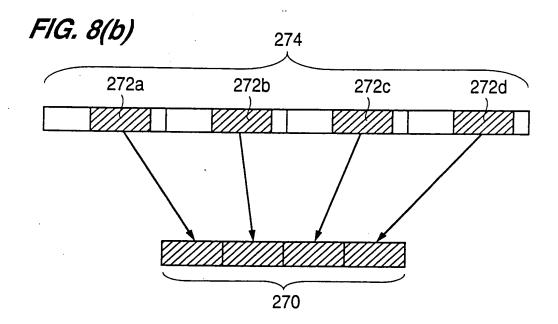






APPROVED	O.G. FIG.				
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APPROVED O.G FIG.

BY CLASS SUBCLASS

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FIG. 8(c)

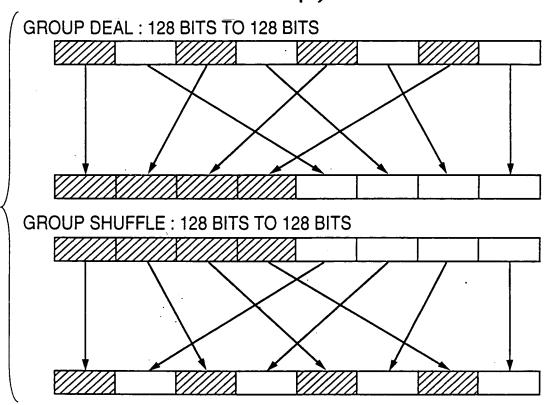
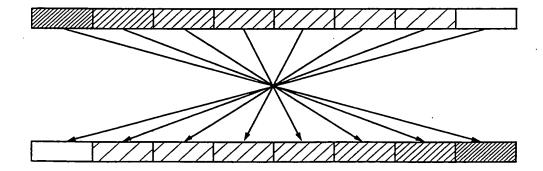


FIG. 8(d)

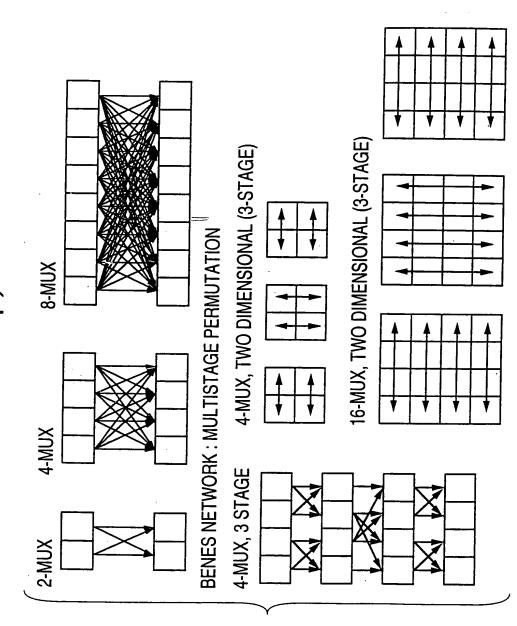


APPROVEU FIG.

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FIG. 8(e)



APPROVED FIG

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FIG. 9(a)

1		31		24	23											0	
			major							im	m						
	28	0	8							2	4						
		31		24	23		18	17								0	
			major			ra						imm					
	28	0	8			6						18					
		31		24	23		18	17		12	11					0	
{			major			ra			rb				im	m			
	28	0	8		•	6			6					2			
		31		24	23		18	17		12	11		6	5		0	
			major			ra			rb			rc			minor		
			8			6			6			6			6	<u></u>	2
		31		24	23		18	17		12	11		6	5		0	
			major			ra			rb			rc			rd		
	28	0/	8			6			6			6			6		

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significand 112 significand 25 significand significand ೫ 9 single half 14. 10.9 112 111 quad sign exponent 52 51 23 22 15 exponent ω exponent exponent 8 5 sign 31 62 sign 83 126 sign 127

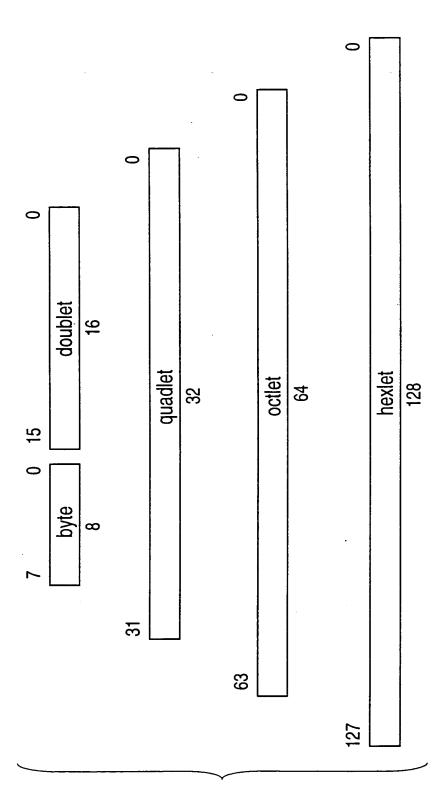
0

FIG. 9(b)

APPROVED 3.

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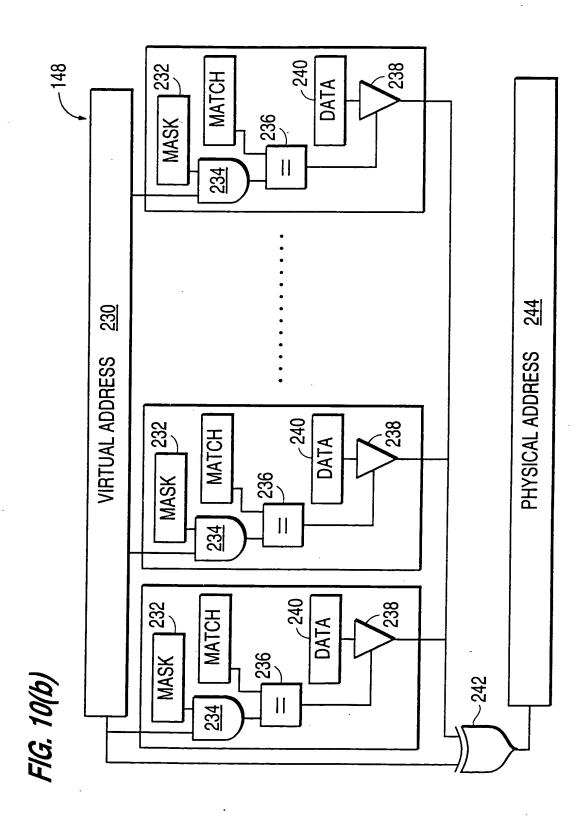
FIG. 9(c)



APPROVED O.G. FIG.

BY CLASS SUBCLASS

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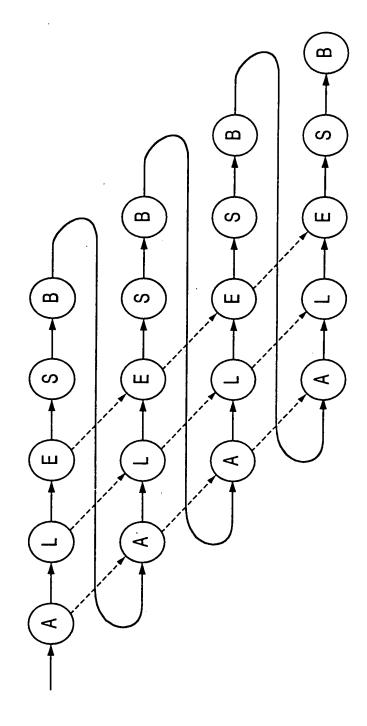


APPROVED O.G. FIG.

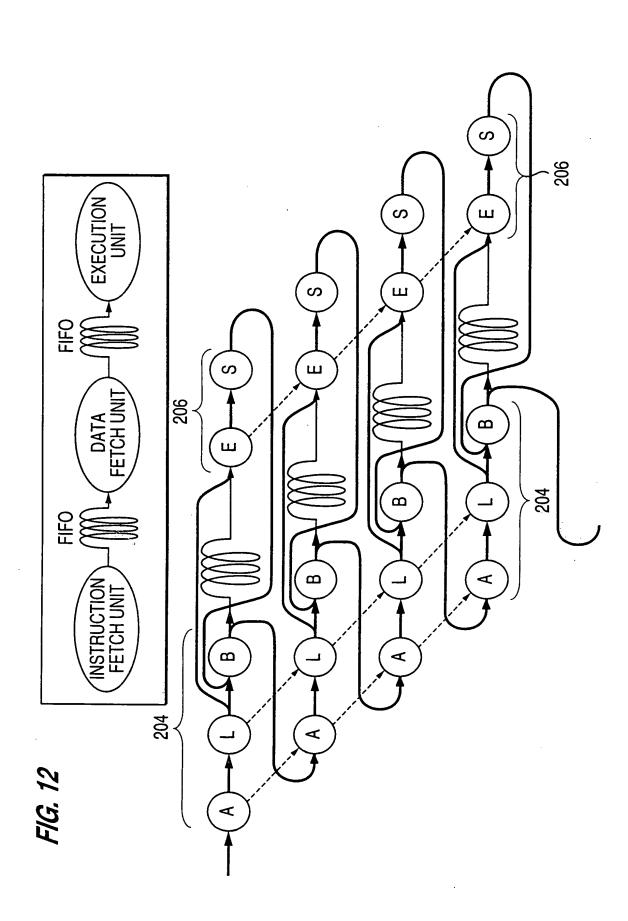
BY CLASS SUBCLASS

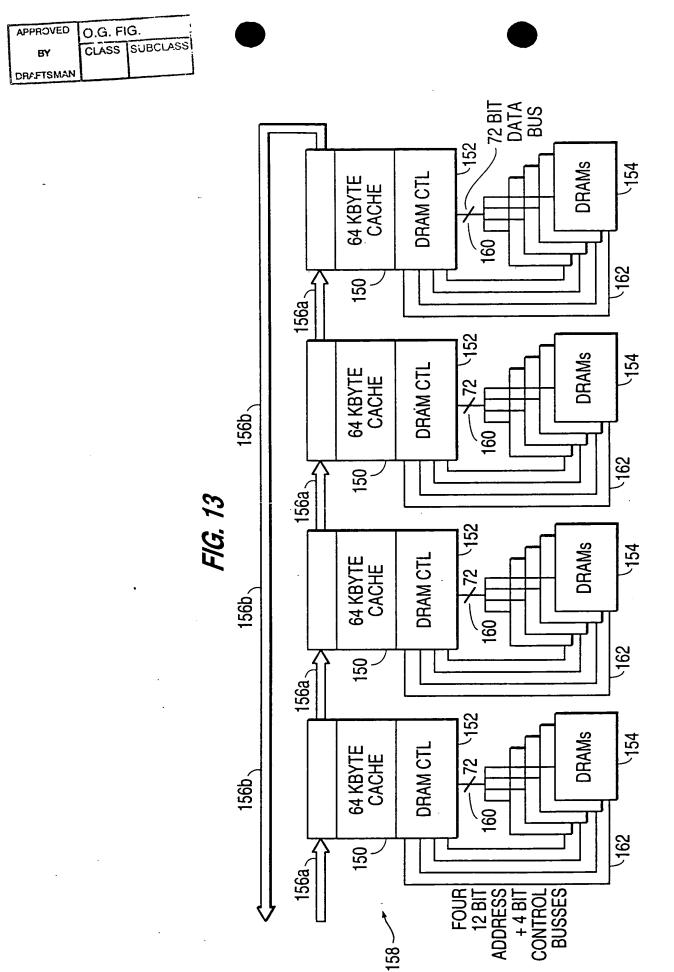
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FIG. 11



•	O.G. FIG.			
BY	CLASS SUBCLASS			
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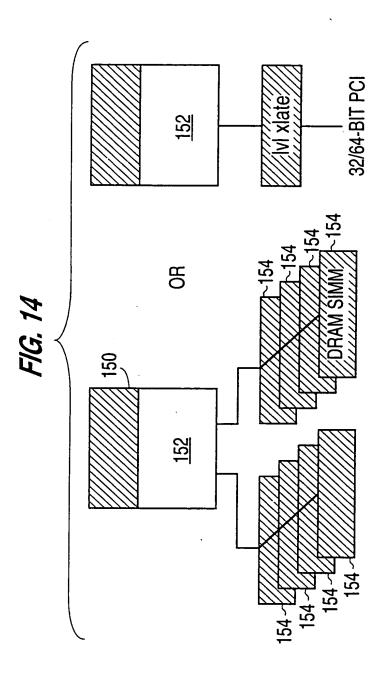




APPROVED O.G. FIG.

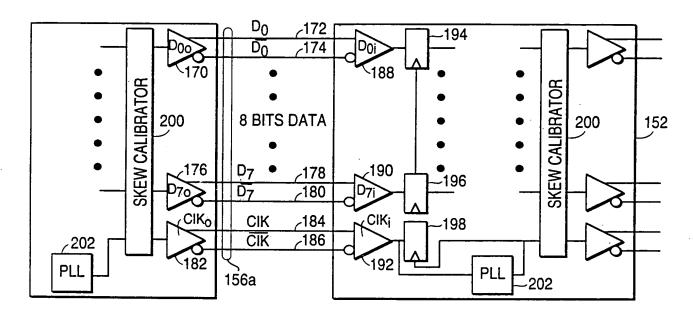
BY CLASS SUBCLASS

DRAFTSMAN



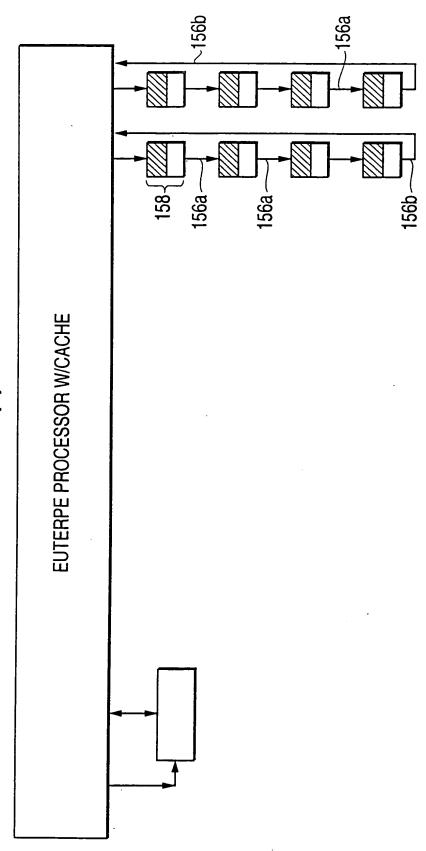
APPROVED	O.G. FIG			
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FIG. 15



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FIG. 16(a)



CLASS SUBCLASS DEVCERSE ВY DRAFTSMAN 3 I/O CHANNELS 214 7 12 208~ 226~ 218 9TH RING FOR MP MICROPROCESSOR W/CACHE 218 FIG. 16(b) 8 MEMORY CHANNELS 4 HIBRAM/RING 210

